

# Front-end ASIC for High Resolution X-Ray Spectrometers

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## I. INTRODUCTION

The work presented here is part of a joint effort between Marshall Space Flight Center (MSFC) and Brookhaven National Laboratory (BNL) to develop a prototype of high-resolution X-Ray Spectrometer (XRS) capable of measuring the abundances of light elements fluoresced by ambient radiation. The XRS is intended in the first instance for elemental mapping of the lunar surface on a near future Lunar Reconnaissance Orbiter (LRO) mission [1], and in the second instance for elemental mapping of the Jupiter's moon Europa on a future Europa Geophysical Explorer (EGE) mission [2]. High priority objective of the LRO mission is to make high spatial resolution global resources assessment including elemental composition, mineralogy, and regolith characteristics [3], and of the EGE mission is to examine the surface composition and search for possible landing sites. Both the LRO and EGE missions are supported by the National Aeronautics and Space Administration (NASA).

The LRO application requires a detector with a  $500 \text{ cm}^2$  area capable of providing an energy resolution better than  $170 \text{ eV}$  at  $2 \text{ keV}$  for rates up to few thousand of counts  $\text{s}^{-1} \text{ cm}^{-2}$  in a power budget of  $20 \text{ mW cm}^{-2}$ . The EGE application requires a detector with similar area capable of providing an energy resolution better than  $130 \text{ eV}$  at  $280 \text{ eV}$  for rates up to one million of counts  $\text{s}^{-1} \text{ cm}^{-2}$  in a power budget of  $80 \text{ mW cm}^{-2}$ . Detector cooling, not included in the power budget, can be provided in both applications for operation down to  $-35 \text{ }^\circ\text{C}$ .

The stringent requirements on area, resolution, rate, and power suggest either the use of standard Silicon diodes with high pixelation (area of few hundred  $\mu\text{m}^2$ ) and bump-bonded front-end electronics or the use of Silicon Semiconductor Drift Detectors (SDDs) [4], [5] with moderate pixelation (area of few tens of  $\text{mm}^2$ ) and wire-bonded front-end electronics. The solution based on SDDs appears more attractive due to the reduced complexity in the readout electronics and the reduced charge sharing, which decreases in a first approximation with the square root of the pixel area [6], [7].

Promising results in terms of rate and resolution were reported by other research groups using pixelated SDDs with the input transistor (e.g. JFET) integrated in each pixel [8-13]. However, the integration of the FET imposes an additional technological challenge, a lower limit in the power dissipation (some  $\text{mW}$  in the JFET itself), and a higher complexity in the front-end electronics and interconnects in order to achieve the required stability, especially at high count rates [14-20].

We propose an XRS prototype based on a pixelated SDD operated without the integrated FET. The anodes of an array of SDD pixels are directly wire-bonded to the inputs of a very low noise multi-channel Application Specific Integrated Circuit (ASIC) here presented.

In Section II of this summary the detector architecture is introduced, and in Section III a brief description of the ASIC and

some preliminary experimental results are reported. Details on the low noise design criteria and architecture of the ASIC will be presented, and the results from the experimental characterization without and with the sensor will be reported. The overall detector architecture, including the interconnection of the ASIC to the SDD pixels, will be also discussed.

## II. DETECTOR ARCHITECTURE

The sensor is composed of hexagonal pixels, each having an area of  $15 \text{ mm}^2$ . Each pixel behaves like an independent, small n-type drift detector with central collecting anode. The drift field, parallel to the sensor surface, is generated using a spiral geometry similar to the ones proposed in [21] and [22]. The anode of each pixel is wire-bonded to the input of a 14-channel ASIC. The electrons generated by the ionizing event are collected in the anode and read out by the ASIC, which provides very low-noise charge amplification, filtering with stabilization, discrimination, peak detection, and multiplexing.

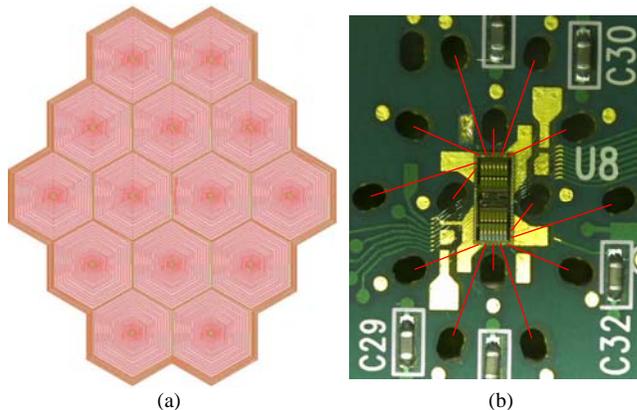


Fig. 1. (a): layout of the unit of 14 SDD pixels and (b) photo of the interposer with the ASIC, where the holes for wire-bonding (traces in red) the inputs to the SDD anodes can be observed.

In Fig. 1(a) the layout of a unit of 14 SDD pixels is shown. The central anodes are wire-bonded to the 14 inputs of the ASIC through holes in an interposer, shown in Fig. 1(b). The interposer also accommodates the interconnections for the biasing and the read out of the ASIC, and for the biasing (three voltages) of the SDD sensor. The resulting 14 - element unit can be tiled to cover an arbitrarily large sensitive area.

## III. ASIC ARCHITECTURE AND PRELIMINARY RESULTS

In Fig. 1 a simplified schematic illustrating the ASIC architecture is shown. In a size of  $2 \times 4.6 \text{ mm}^2$  and a power budget of  $1.6 \text{ mW / channel}$  the ASIC includes 14 front-end channels, multiplexers, bias circuitry, registers, DACs, and readout logic.

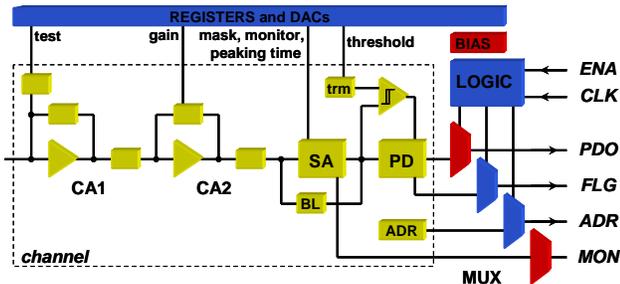


Fig. 1. Simplified schematic illustrating the ASIC architecture.

The charge amplifier is a dual stage (CA1, CA2) with adaptive compensated continuous reset similar to the one described in [23], [24] and charge gain adjustable to either 1024 or 341. An innovative aspect of this realization is the use of MOSFETs in place of the capacitors (i.e. MOSFET-only feedback), with linearity recovered by the compensation effect. The charge amplifier input MOSFET operates at a drain current of 200  $\mu\text{A}$  and it is optimized for an input capacitance of 200 fF [25]. It follows a 5<sup>th</sup> order shaper [26] (SA) with peaking time adjustable to 0.5, 1, 2, and 4  $\mu\text{s}$  and with output baseline stabilized using a band-gap referenced BLH circuit [27] (BA). The overall channel gain can be adjusted to either 1.15 or 3.45 V/fC, covering an energy range up to 12 keV and 36 keV respectively. A low-hysteresis comparator with multiple-firing suppression provides event discrimination controlled with a 10-bit DAC common to all channels and an on-channel 3-bit DAC for equalization. Above threshold events are processed by a two-phase peak detector with analog memory [28] (PD). A flag (FLG) indicates a successful acquisition ready to be read out. At each clock (CK) the peak amplitude (PDO) and the address (ADR) of all above threshold events are made sequentially available at dedicated outputs, thus providing sparsification. The readout process makes use of both CMOS and Low Voltage Differential Signaling (LVDS). Additional functions include channel mask, channel test capacitor, on-chip test pulse generator with amplitude controlled by a 10-bit DAC, pixel leakage current measurement circuitry (gain  $\approx 1$  mV/pA), monitor (MON) of channel shaper outputs and DAC voltages, and an optional acquisition-disable function either at pulse threshold crossing or at pulse peak.

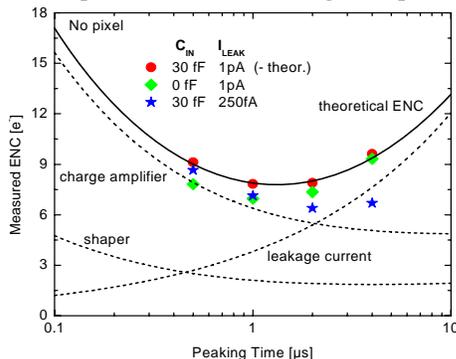


Fig. 2. Measured ENC without pixel for different cases of external input capacitance  $C_{IN}$  and leakage current  $I_{LEAK}$ . The theoretical ENC for the 30fF, 1pA case is also shown, along with the dominant contributions.

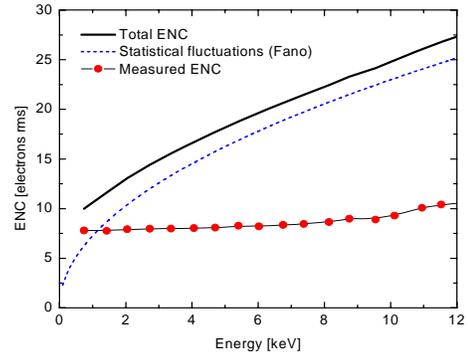


Fig. 3. Measured ENC vs injected charge (energy equivalent in Si), simulated contribution due to statistical fluctuations (Fano limited), and total ENC.

In Fig.2 the measured ENC is shown for cases without pixel and with external input capacitance  $C_{IN} \approx 0$  fF and  $\approx 30$  fF, and input leakage currents  $I_{LEAK} \approx 250$  fA and  $\approx 1$  pA. The theoretical ENC for the 30 fF, 1 pA case is also shown along with the contributions from the charge amplifier, shaper, and leakage current. Only the contribution from the charge amplifier increases with  $C_{IN}$ . An ENC below 12  $e^-$  is expected with the SDD pixel connected and cooled below  $-10$   $^{\circ}\text{C}$  (i.e.  $\approx 110$  eV at 280 eV in Si). In Fig. 3 the increase of the ENC with the injected charge  $Q_{IN}$  (energy equivalent in Si) for the 30 fF, 1 pA case is shown. This effect is due to the discharge from the continuous reset [23] and it appears negligible when compared with the statistical fluctuations in the charge generated by the ionizing events, also simulated in Fig.3.

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